01P 73707

58

(12) UK Patent Application (19) GB (11) 2 136 569 A

(43) Application published 19 Sep 1984

(21) Application No 8405724

(22) Date of filing 5 Mar 1984

(30) Priority data

(31) 8306134 (32) 5 Mar 1983 (33) GB

(71) Applicant
Robert Joseph Savage,
"Ulverley", Woodland Way, Kingswood, Surrey

(72) Inventor
Robert Joseph Savage

(74) Agent and/or Address for service
J. A. Boutland,
8 Heatherstone Avenue, Hythe, Southampton SO4 5LQ

(51) INT CL[3]
G01N 29/04

(52) Domestic classification
G1G 2 4C 4E 7T PC

(56) Documents cited
GB 1579651
GB 1549667
GB 1543311
GB 1402495
GB 1332898
GB 0699796
EP A2 0073893
"Ultrasonic Testing of Materials" by Krautkramer, 2nd Ed, Springer-Verlay 1977. eg Chapters 10 and 16.

(58) Field of search
G1G

(54) Testing of structures

(57) A method of testing a structure for the presence of a crack (12) or other fault, comprises applying an energy pulse (10*b*) to the structure, for example by use of hammer (11), and sensing energy of a pulse (10*c*) reflected from the crack (12) by use of an accelerometer (13). Initiation of the sensing may be delayed for a predetermined period after application of the energy pulse (10*b*), so as not to include a direct pulse (10*a*) passing directly to the accelerometer (13). The sensed signal is fed by way of an integrator to a display meter.

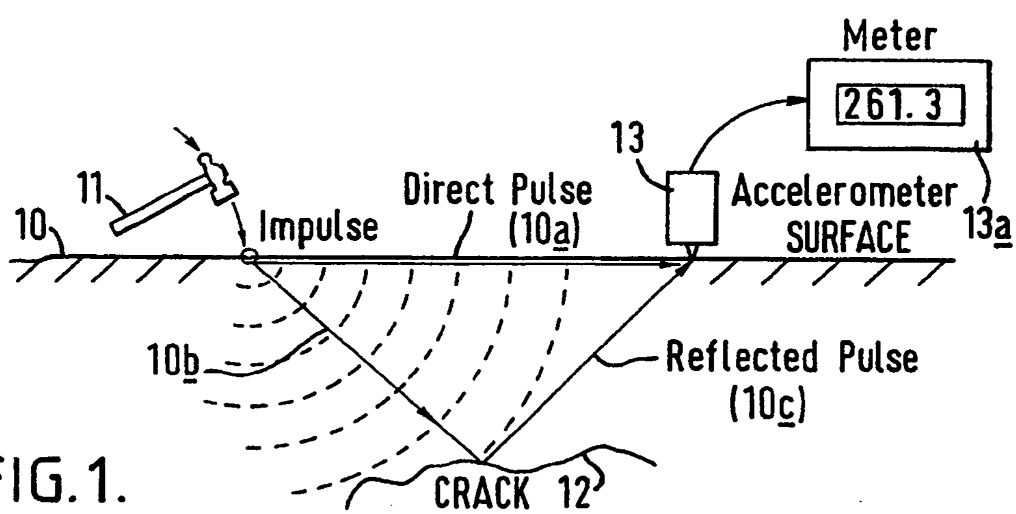


FIG. 1.

GB 2 136 569 A

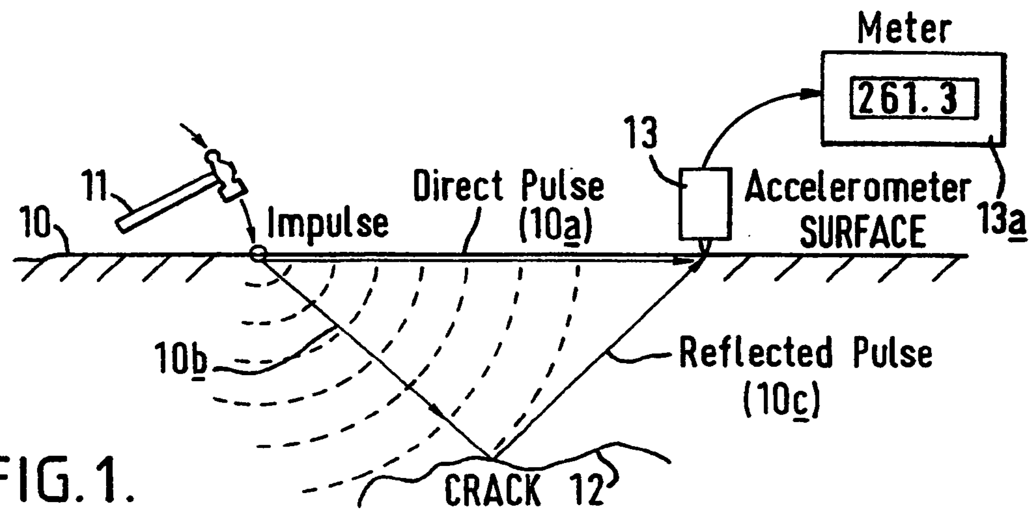


FIG. 1.

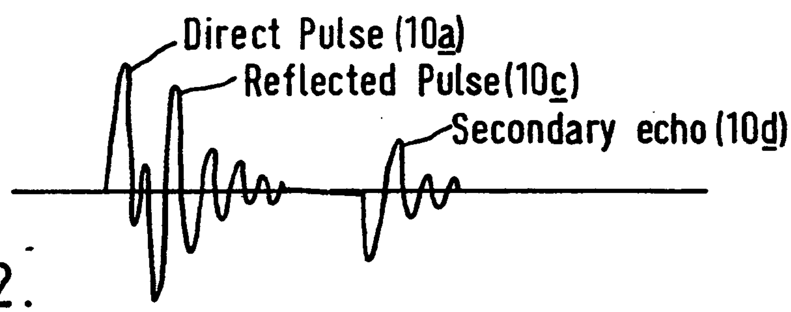


FIG. 2.

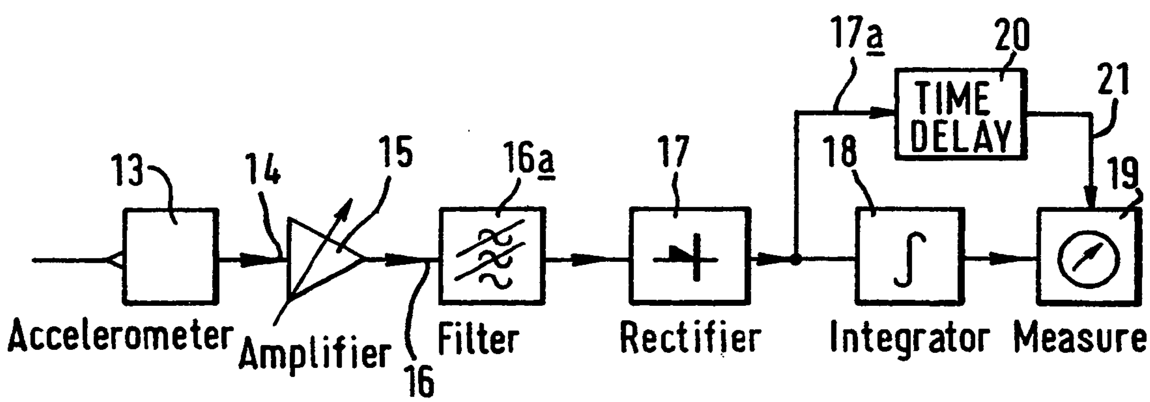


FIG. 3.

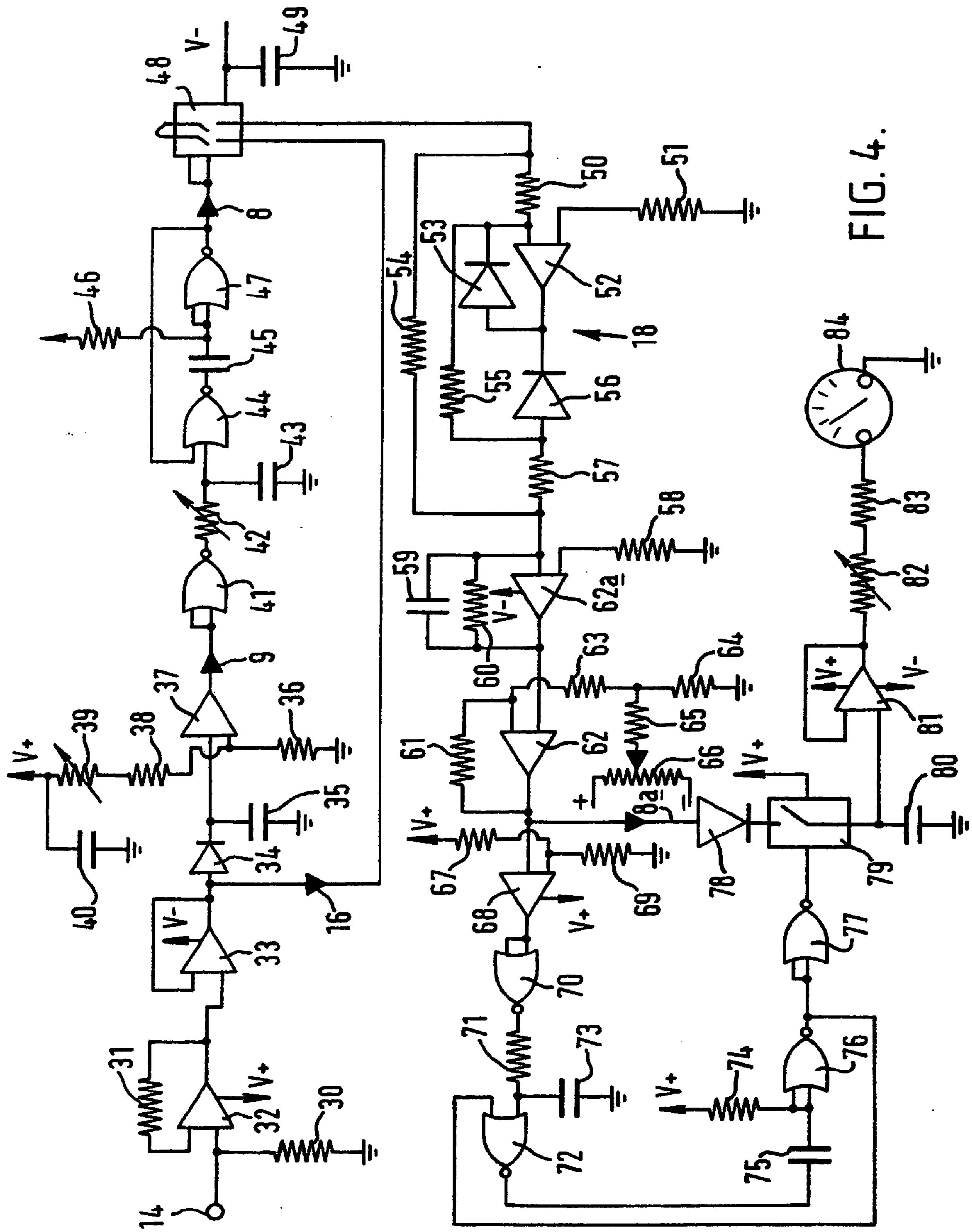


FIG. 4.

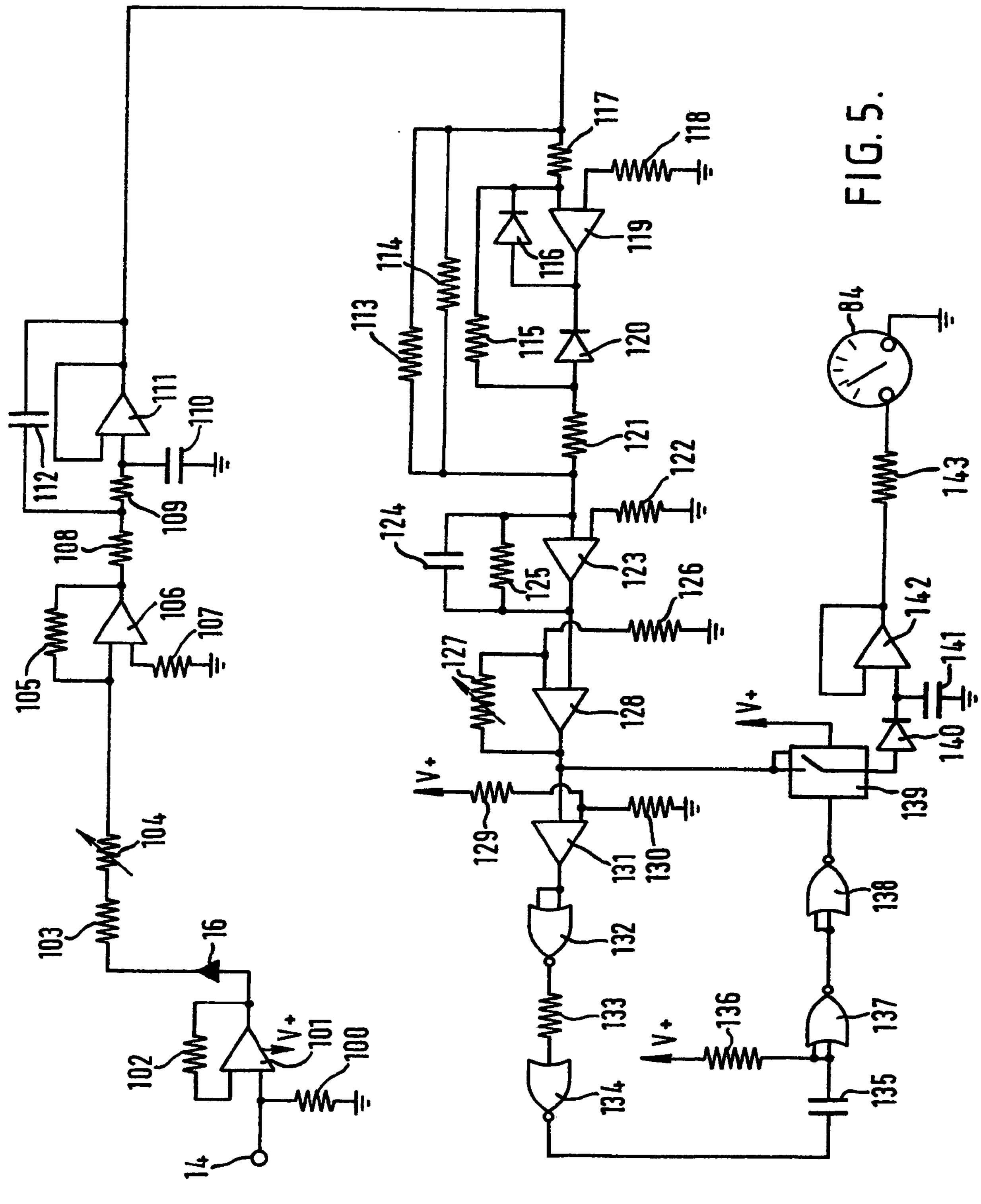

14
100
101
V+
102
16
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
V+
129
130
131
132
133
134
V+
135
136
137
138
139
V+
140
141
142
143
84

FIG. 5.

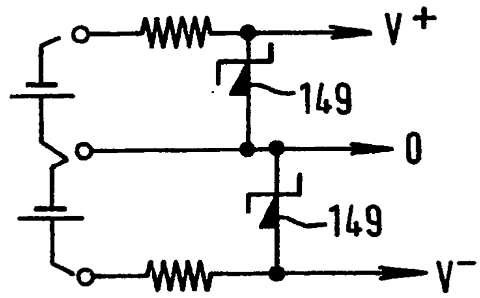


FIG. 6.

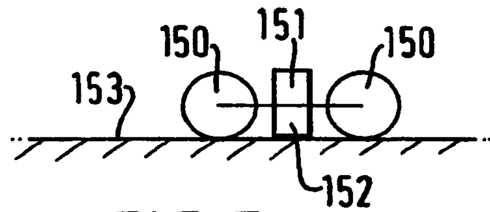


FIG. 7.

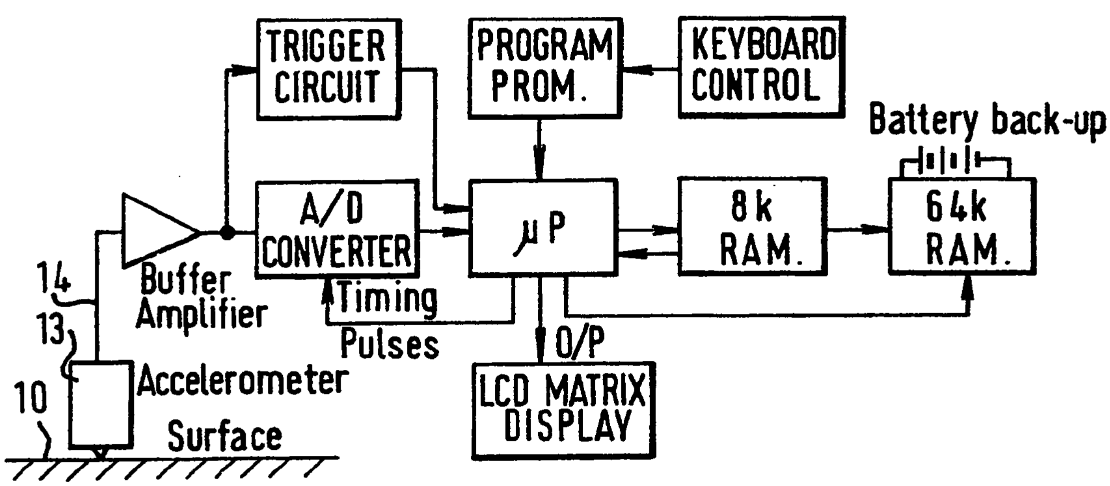


FIG. 8.

FIG. 9.

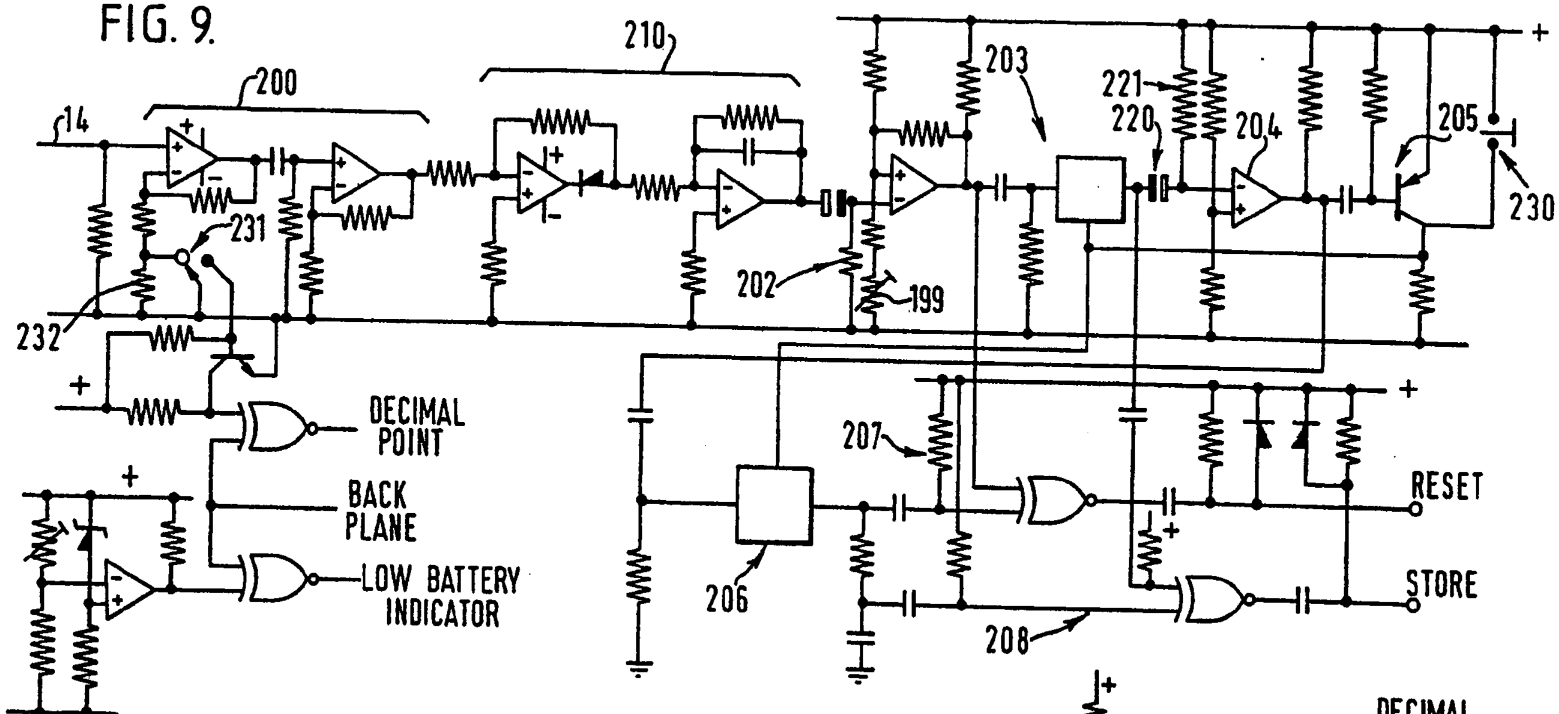
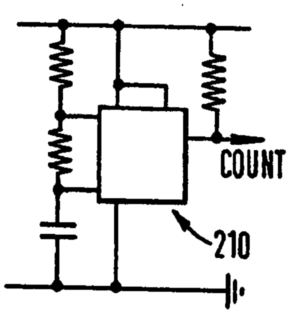


FIG. 10.



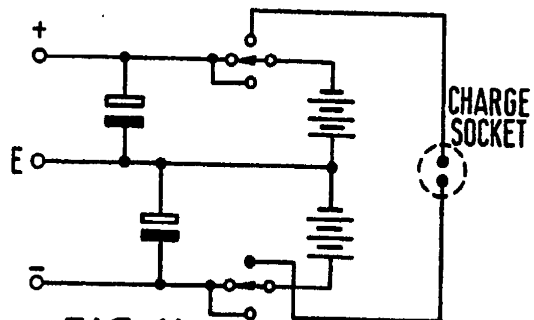


FIG. 11.

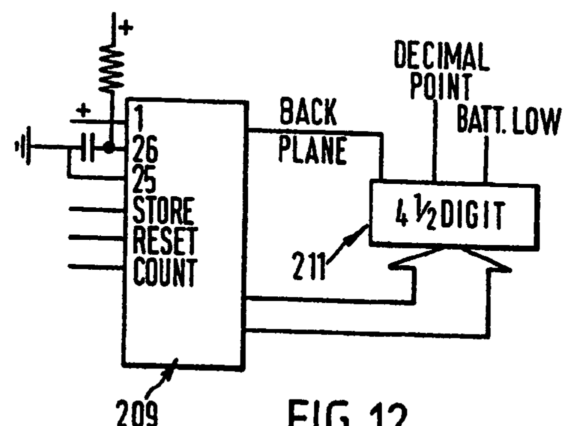


FIG. 12.

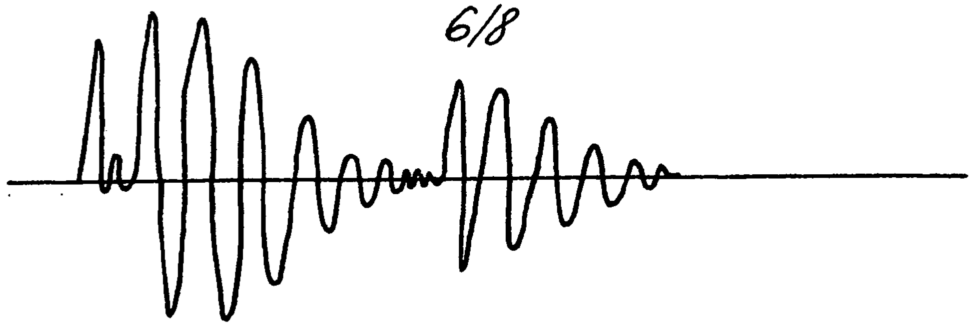


FIG. 13. Waveform from a large Anomaly.

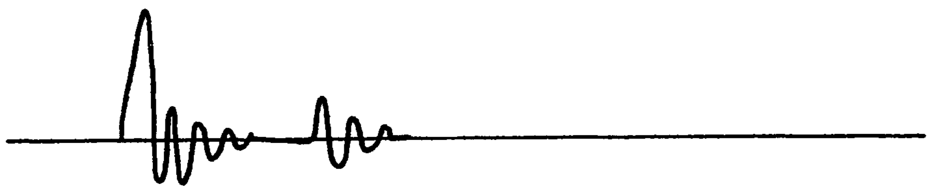


FIG. 14. Waveform from a flawless structure.

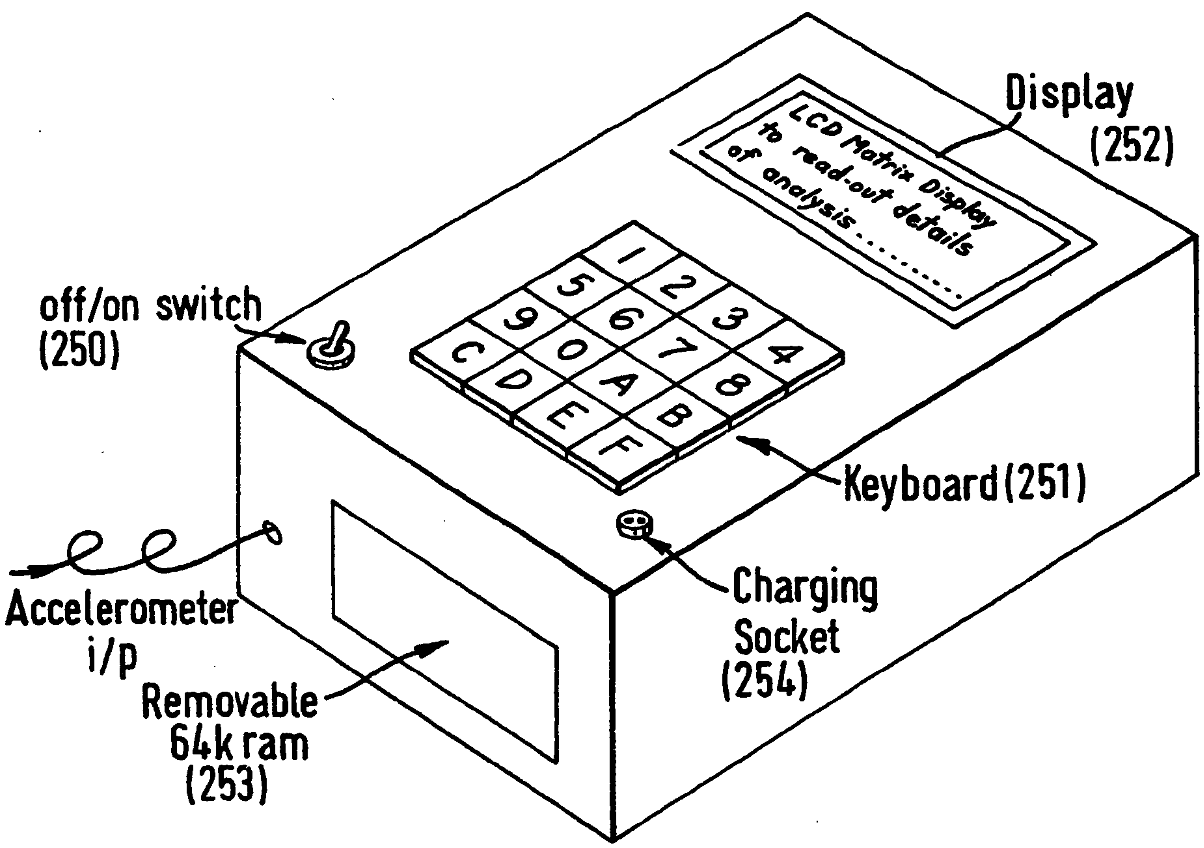


FIG. 16. COMPLEX SYSTEM LAYOUT.

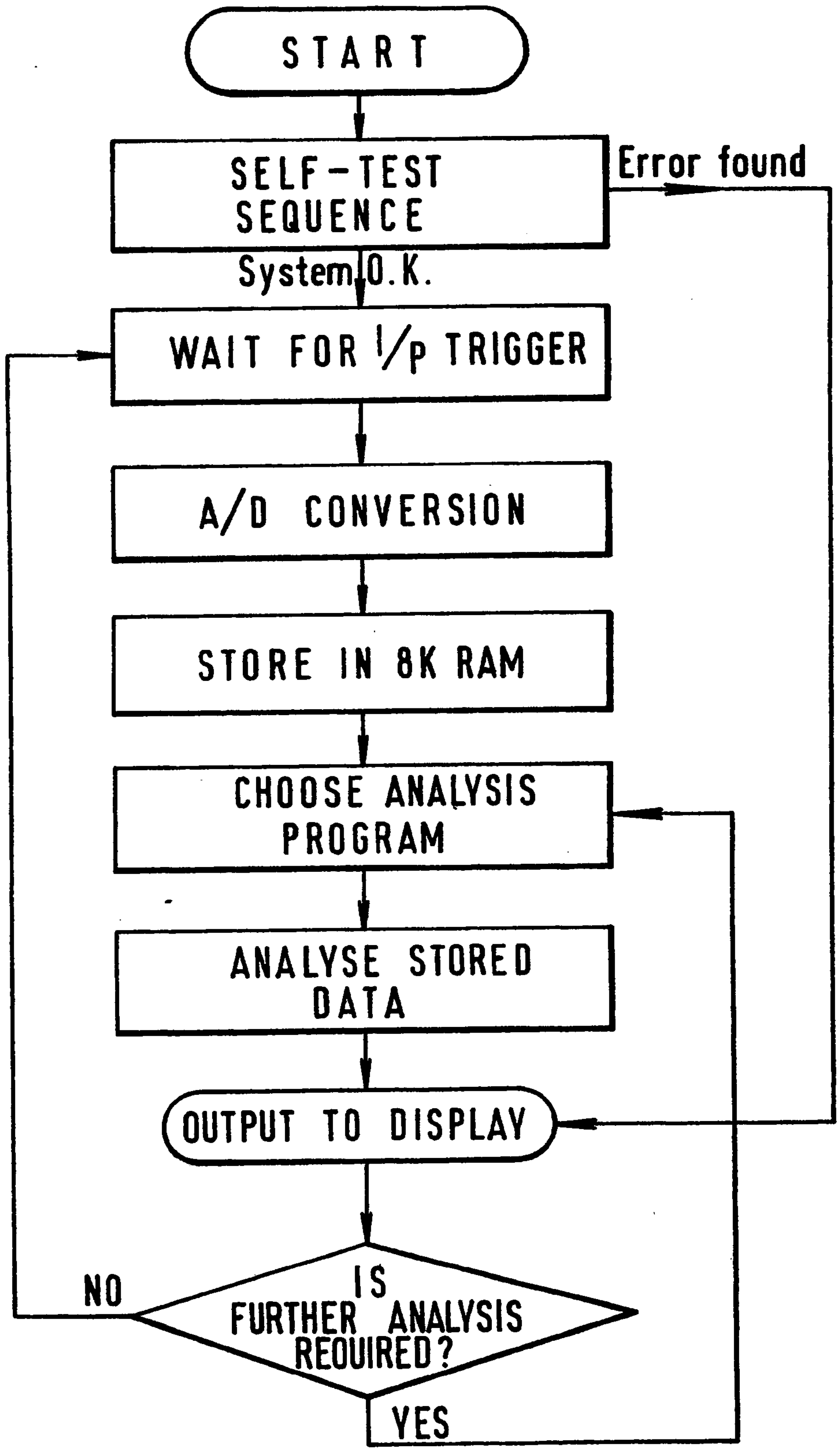


FIG. 15. TYPICAL FLOW DIAGRAM.

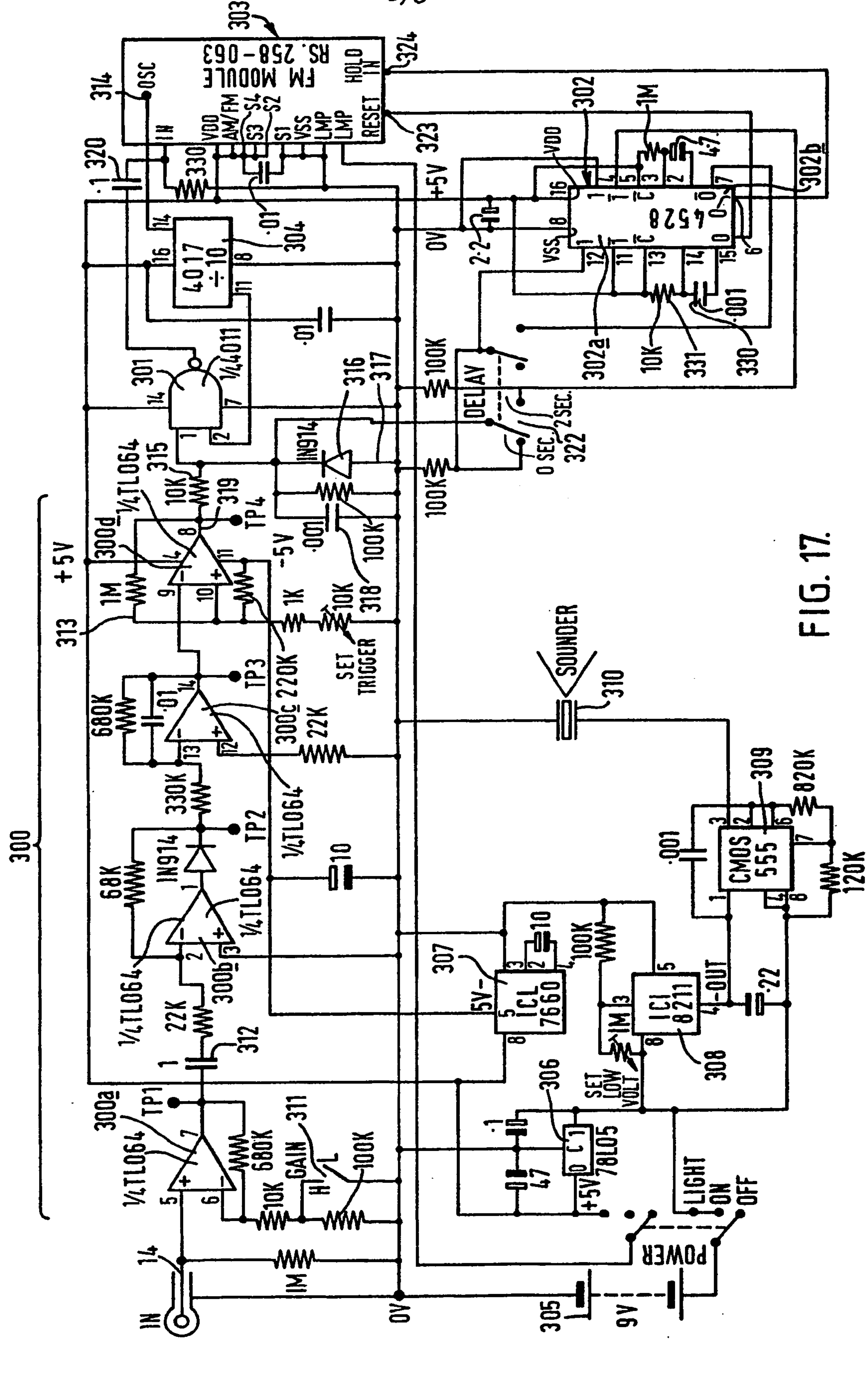

FM MODULE
RS. 258-063
DELAY
SOUNDER
CMOS 555
ICL 7660
ICL 8211
4017 ÷10
4528
1/4 4011
1/4 TL064
78L05
SET TRIGGER
SET LOW VOLT
GAIN
POWER
LIGHT ON OFF
IN
0V
+5V
-5V
9V

FIG. 17.

SPECIFICATION

Improvements in or relating to the testing of structures

Background of the invention

This invention relates to the testing of structures.

It is desirable to be able to test structures for faults, anomalies or irregularities, (hereinafter collectively referred to as faults), which are not readily visible.

Summaries of the invention

According to one aspect of the invention, a method of testing a structure comprises applying an energy pulse to the structure, and sensing energy of said pulse reflected from a fault in the structure.

The method may comprise the step of delaying the initiation of said sensing for a predetermined period after application of said energy pulse.

Said sensing may include forming an electrical signal, integrating said signal, and displaying the integrated signal.

Said electrical signal may be used to obtain a time delay signal for causing said display to cease after a predetermined display time.

In one method, the electrical signal is produced by an accelerometer, the signal is rectified, the rectified signal is fed to a normally open switch device and to a first time-delay device which after a first predetermined time triggers a second time-delay device to close the switch device, the second time-delay device opening the switch device after a second predetermined delay.

The rectified signal may pass from the switch device through an integrator to a display meter through a further switch device. The integrated signal may pass to a third time-delay device arranged to open the further switch device after a predetermined time and close the further switch device after a further predetermined time, closing of the further switch device being arranged to return the meter to a datum position. The method may comprise deriving from said integrated signal a measure of the energy in the integrated signal. The measure may be displayed digitally.

According to another aspect of the invention, apparatus for testing a structure comprises means for applying an energy pulse to the structure, and means for sensing energy of said pulse reflected from a fault in the structure.

The apparatus may be provided with means for delaying the operation of said sensing means for a predetermined period after said pulse is applied.

One embodiment comprises accelerometer means for producing an output signal, integrator means operable to receive the output signal after a time delay and produce an integrated signal, and display meter means for displaying the integrated signal.

The apparatus may comprise switch means for receiving the integrated signal; time-delay means arranged to open said switch means when said integrated signal has passed therethrough, and then to close said switch means after a predetermined time, said time-delay means being operable so as to be responsive to said integrated signal.

The apparatus may comprise further time-delay means arranged to receive the output signal from the accelerometer, a normally open switch means operable so as to receive this signal, another time-delay means which after a first predetermined time controlled by the further time-delay means is energized by the further time-delay means and closes the switch means and then opens the switch means after a second predetermined time.

The display meter means may be arranged to provide a digital display.

The apparatus may include means for deriving from the integrated signal, a measure of the energy in the integrated signal.

According to a further aspect of the invention, apparatus for testing a structure comprises means for applying an energy pulse to the structure, means for sensing energy of said pulse reflected from a fault in the structure, and means for measuring the energy in said reflected pulse or in a predetermined period.

According to yet another aspect of the invention, a method of testing a structure comprises applying an energy pulse to the structure, and sensing energy of said pulse reflected from a fault in the structure, said sensing of energy comprising means for providing a measure of energy in the reflected pulse or in a predetermined period.

Brief description of the drawings

The invention may be performed in various ways and three specific embodiments with possible modifications will now be described by way of example, with reference to the accompanying drawings, wherein :-

Figure 1 is a schematic view of apparatus being used to test for faults such as cracks or voids,

Figure 2 illustrates one waveform,

Figure 3 is a block diagram of one form of apparatus,

Figure 4 is a circuit diagram for one form of apparatus,

Figure 5 is a circuit diagram for another form of apparatus,

Figure 6 shows a modification for Figure 4,

Figure 7 shows the apparatus in association with a device for measuring distance on a surface,

Figure 8 is a schematic view of another apparatus.

Figure 9 is a circuit for a digital display,

Figure 10 is an oscillator circuit,

Figure 11 is a battery circuit,

Figure 12 is a display section,

Figures 13 and *14* show other waveforms,

Figure 15 shows a flow or operational sequence,

Figure 16 shows a hand-held instrument, and

Figure 17 is a circuit diagram for a third form of apparatus.

Detailed description of the preferred embodiments

If a transient impact, for example a blow from a hammer arrangement, is delivered to a plane surface of a structure, a hemispherical compression or *p* wave travels downwardly and outwardly into the structure from the point of impact, with diminishing amplitude with respect to the distance travelled. If

the *p* wave meets a fault such as a crack or void in the material of the structure, reflection waves are initiated and returned to the plane surface at the same velocity as the original *p* wave. If an acceleration or velocity sensor is placed on the surface near the impact point, the sensor will pick up the reflection waves from the crack or void. These reflection waves will continue for a time, and energy will be received by the sensor for a much longer time than in the case where the material has substantially no faults, e.g. cracks or voids. Thus consideration of the length of time the sensor is receiving reflection waves can provide a user with a qualitative knowledge of the state of integrity of the surface and interior under inspection.

This general arrangement is shown in Figure 1 where a plane surface 10 of a structure receives a single blow from a hammer device 11. The resulting compression wave 10*b* travelling downwardly and outwardly into the structure from the point of impact hits a fault comprising a void or crack 12, and the reflection wave 10*c* initiated is received by an accelerometer 13 disposed on the surface 10, adjacent the hammer device 11. The *p* and reflection waves (10*b* and 10*c* respectively), are not of a single frequency.

The accelerometer 13 is attached firmly to the surface 10 under test, and its output connected to a measuring system 13*a* comprising a meter. The acoustic waves produced by the hammer blow impulse travel as two main parts, namely a surface wave or direct pulse 10*a* which goes directly to the accelerometer 13 and a compression or *p* wave which goes down into the material of the structure and is reflected by any discontinuity in the material. Thus, the signal output of the accelerometer is of the general form shown in Figure 2, comprising a direct pulse 10*a*, followed by a reflected pulse 10*c*, and then a series of secondary echoes 10*d*.

The meter or measuring system 13*a* is adjusted to measure the amount of energy contained in the reflected pulse 10*c*, plus the energy in the secondary echoes 10*d* above a certain predetermined threshold level. If this energy is large it can be assumed that the discontinuity which reflected it is also large. If it is small, it can be assumed that the structure is either sound, the discontinuity is small, or that the reading was caused by small irregularities in the otherwise homogeneous material, such as the pebbles in concrete. (Or rivets in a steel structure).

Typically on a sound concrete structure a reading of 90-150 is obtained when meter 13*a* is in a low gain mode. Where a crack or like fault is within 0.5 metres of surface 10 of the structure, a reading of 5000-10000 can be expected.

The invention is particularly applicable to the testing or inspection of concrete walls and floors for cracks or de-laminations, and these are structures which can be tested, but the invention may be used in the testing of other surfaces and structures.

One form of apparatus for use in the invention introduces a pulse of energy into the structure and then measures the amount of reflection occurring in a fixed time.

The structure may exhibit resonance in response to the *p* wave.

The method used is to integrate the signal from an accelerometer attached to the structure and display the result on either an anologue or digital meter. In order not to include the actual initial or direct impulse energy, a short predetermined time delay is incorporated before the integration process starts. The block diagram of Figure 3 shows the basic system. However, energy sensing delay need not be provided for if the energy of the direct pulse 10*a* is small compared with the energy of the reflected pulse 10*c*. In such cases the added effect of pulse 10*a* is acceptable.

With reference once more to Figure 3, the incoming signal at 14 from the accelerometer 13 is first buffered by buffer amplifier 15 to produce a signal 16 which is then passed through a filter 16*a* to a rectifier 17. The rectifier 17 removes the initial millisecond of response, thus disregarding the shear and Rayleigh wave signals caused by the disturbing pulse itself. The remaining signal is integrated in an integrator 18 and displayed on an analogue or digital meter 19 (which corresponds to meter 13*a*). At the same time, a further time delay is generated by time-delay system 20 from the output 17*a* from rectifier 17. At the end of this further delay, the display in meter 19 is reset to zero through a connection 21. The time-delay of rectifier 17 can be varied. For example, it can be two milliseconds.

Hammer 11 (Figure 1) is preferably provided with a choice of heads, so as to suit the type of structure being investigated. Thus heads of steel, brass and hard plastics material are suitable for, respectively, concrete, steel and wood.

Two practical embodiments of the system are shown in the circuit diagrams of Figures 4 and 5. These embodiments are preferably portable and battery operated.

Referring to both Figures 3 and 4, the accelerometer output signal 14 is buffered by buffer amplifier 30-33. The initial time delay is generated by rectifying the buffered accelerometer signal 16 by diode 34 and applying it to a comparator 35-40 presettable by variable resistor 39. The higher the comparator setting, the longer the time before the comparator switches to produce an output 9. The comparator output 9 is used to trigger another timing circuit 41-47, set by variable resistor 42 to about 12 milliseconds. The output 8 of the timing circuit 41-47 switches a normally open analogue switch 48 "on" after the initial first delay produced by the comparator, and then off again about 12 milliseconds later. The buffered accelerometer signal 16 passes directly through this switch 48 to the integrator circuit 50-66. Thus, these two timing circuits ensure that an accurately measured period of signal is passed to the integrator 18. Energy sensing delay is provided by circuit components 42 and 43.

The integrator 18 comprises a simple full-wave rectifier system 50-57 followed by an operational amplifier integrator including amplifiers 62, 62*a*.

The integrator output 8*a* passes to a rectifying diode 78 and through a further analogue switch 79 to a buffer amplifier 81, resistors 82, 83 and a display meter 84. (Meter 84 corresponds to meter 19 of

Figure 3). The integrated signal value is stored on a capacitor 80 connected to switch 79 and amplifier 81. At the same time, the integrated signal 8*a* passes to a further time delay system 67-77 which opens the analogue switch 79 after the integrated signal 8*a* has passed through the switch 79, and then shuts it again about 3 seconds later. The closing of this analogue switch 79 discharges the capacitor 80, thereby allowing the display meter 84 to return to zero.

The circuit of Figure 5 is generally similar to that of Figure 4, except that the first two timing delay circuits and the analogue switch 48 are replaced by a low pass filter system 103-112 achieving the same result, making use of the fact that the direct wave is of lower frequency than the reflected wave. Parts 100 to 102 forming a buffer amplifier.

The signal from the low pass filter system is again rectified by system 113-121 and integrated by system 122-128. The integrated signal passes to delay circuit 129-138 and to analogue switch 139 and is rectified by diode 140. The rectified signal is stored in capacitor 141, buffered by amplifier 142 and passes to the display meter 84 through resistor 143. As in the circuit of Figure 4, the meter is returned to zero by the delay circuit 129-138 closing the switch 139. In some circumstances the filter is not an adequate substitute for the positive time-delay device as the filter only attenuates the direct pulse 10*a* (Figure 1) and does not fully remove it.

Figure 6 shows a modification for Figure 4, in which Zener diodes 149 are used to produce an accurately stabilized power supply.

The circuits described above can be improved to reduce their power consumption by using micro-power operational amplifiers, a single rail power supply, and a more economical comparator.

The analogue meter display can be replaced by a liquid crystal display (LCD) system, if required, or the data can be stored digitally for later processing.

It will be appreciated that to obtain successful results, impacts in the same series of test must be applied with substantially uniform force and at substantially uniform distance from the accelerometer.

Figure 7 shows one possible use of the apparatus. A trolley has wheels 150 which are associated with a mechanism 151 for indicating the distance travelled along the ground surface 153, for example a road. The trolley carries testing apparatus 152 arranged to apply an impulse of energy to the road as required and to measure the amount of reflected energy in a predetermined time. Thus the condition of the road can be tested whilst measuring distances along the road.

The trolley may be self-propelled, comprising for example, a motor vehicle whereby testing can be carried out at speed.

Information obtained from testing can be recorded, for example, on tape, which can subsequently be fed into a computer.

In a preferred arrangement shown in Figures 8 to 12, the meter read-out is a 4 digit LCD driven by a 7224 integrated circuit. A pulse train is switched on by the leading edge of the integrated energy waveform, and switched off when that energy waveform has decayed to a predetermined level. The number of pulses counted by the 7224 is therefore a direct measure of the energy contained in the waveform. No significant delay of energy sensing is provided for.

The system can use very low power consumption devices and may for example, run for over 200 hours between battery charges.

The accelerometer output signal 14 is amplified by a 7621 operational amplifier 200, and rectified and integrated by another 7621 operational amplifier 201. The output from the integrator feeds to a Schmidt trigger circuit (1/4 of an LM 339) 202 and the output of that trigger circuit is used to trigger an RS flip-flop bistable integrated circuit (1/4 of a 4043) 203. The trigger can be adjusted by resister 199. The output of the bistable feeds to another section 204 of the LM 339 which is adjusted to act as an ordinary comparator. Its output feeds to both a PNP transistor 205 (type BC 214) and to another section 206 of the 4043 bistable integrated circuit. The output of this bistable feeds to two sections 207, 208 of a 4077 exclusive NOR circuit. The circuit action is as follows :-

The incoming accelerometer signal is amplified, rectified and integrated so that the output signal from the integrator is a positive voltage whose duration is proportional to the energy contained in the accelerometer signal. The initial rise of this integrated positive voltage causes the Schmidt trigger to fire, which in turn produces a reset pulse via one section 207 of the 4077. This reset pulse causes a counter in a 7224 digital driver integrated circuit 209, Figure 12, to reset to zero and start counting pulses produced by a 555 oscillator 210, Figure 10, connected to it.

When the integrated positive voltage has decayed sufficiently, (such decay time being determined by the accelerometer energy content), the Schmidt trigger turns off, producing an output signal of the opposite polarity. This second pulse triggers the first 4043, reference 203, which immediately produces an output signal feeding to the second LM 339 section 204 and to the 4077 "store" section 208. This "store" signal feeds to the digital driver circuit 209 and stops its counter, so that the count displayed by a 4½ digit LCD readout 211 represents the time of decay of the integrated signal from the integrator. The signal from the second LM 339 section 204 is determined by a decay time constant dependent on a capacitor 220 and resistor 221 between it and the circuit 203. This time delay is about 3 seconds. At the end of that period, the section 204 generates a pulse which causes the transistor 205 to feed out a "reset" pulse, which resets both the 4043 sections 203, 206 and feeds another reset pulse to the circuit 209 followed immediately by a "store" pulse. Thus, the LCD readout resets to "0", because it does not have time to count between the "reset" pulse and the "store" pulse.

If the total 3 second reading period is not required, the circuit 209 can be reset to zero earlier by using a "Reset" button 230 which generates a reset sequence from the output of the transistor 205.

The gain of the first amplifier 200 can be altered, to allow for very low energy inputs, by mens of a switch 231 connected across resistor 232 which changes the amplifier gain by a factor of 10. At the same time, the decimal point on the digital display is illuminated, so that the readout indicates a reduction of 10 in the accelerometer energy.

Thus, the main differences between this arrangement and those previously described with reference to Figures 4 and 5, is that the readout is digital instead of analogue, and that a truer representation of the accelerometer output is displayed, because the duration of the integrated energy is read out, rather than its amplitude.

It is useful to consider what the complex waveform from the accelerometer represents.

Consider the general statement above that a large readout number indicates a large crack, whereas a small number indicates a lack of discontinuities. It could be equally true that a large number indicates a lot of small cracks, and that a small number could be the result of two similar cracks which sent back reflections which were exactly out of phase, thereby cancelling out.

In fact, the process of integrating the reflected energy, although it gives a good measure of total amplitude, destroys all information relating to phase and secondary echoes. This time-related information must contain a great deal of additional facts which would make analysis easier, if it could be separated and displayed in a fairly simple manner.

If the final display contains words as well as numbers, this will clarify the type of reading for a non-technical operator and remove a lot of the confusion which may occur.

Typical accelerometer output waveforms are shown in Figures 2, 13 and 14.

Figure 2 shows the output caused by a small anomaly.

Figure 13 shows the output caused by a large anomaly.

Figure 14 shows the output caused by no anomaly.

Taking Figure 2 as a guide, in all cases the accelerometer output consists of a direct pulse, followed by a decaying oscillation caused by the reflections from an anomaly, followed by further oscillatory decay waveforms caused, for example, by more distant anomalies or edges of the structure. The greater the size and number of the reflected pulses, the greater the size or number of the anomalies.

However, there is a great deal more information present in the waveform. For example, the time between the leading edge of the direct pulse and the leading edge of the first reflected pulse gives the difference in time (and hence path length) between the surface wave and the reflected wave. It is also probable that the rate of decay of the first reflected pulse train is related to the volume of the anomaly (e.g. a long decay represents a large void and a quick decay represents a narrow crack).

The frequency of the waveform also gives information about the structure. Stiffer structures tend to resonate at higher frequencies, so a large anomaly will not only produce reflections but those reflections will be frequency-shifted, and also phase-shifted.

Thus, information concerning the anomalies in a structure is present in amplitude, frequency, phase, decay time and repetition rate of the accelerometer waveform. It is to consider which of these can be measured with reasonable accuracy and at reasonable cost.

Using a pen recorder, a complete record of any waveform could be made. However, it is difficult and time-consuming to analyse pen recordings. When it is realised that the investigation of a small section of motorway involves taking readings at every crossing of a metre grid, (i.e. about 100 readings for every 10 metre length of motorway), it can be seen that pen recordings could take too long to translate into useful facts, (apart from problems of providing the electric power requirements on site).

An alternative method is a tape recorder. However, this shifts the problem of interpretation from the motorway of the laboratory. The tape recording has to be indexed accurately and then replayed in the laboratory into some form of analyser. As electrical power is readily available in the laboratory, the analyser could be a large and complex computer.

The following discussion is concerned with methods of assimilating and interpreting non-repetitive oscillatory waveforms of the type shown in Figures 2 and 13, and the unambiguous presentation of that information for immediate use.

Analogue to digital conversion

All microprocessor systems are basically digitally operated. Therefore all input signals have to be translated into digital format, and all output signals have to be translated back into either analogue format, or normal arabic numerals.

Analysis of typical waveforms to be expected from the accelerometer show that the minimum time interval between successive crossings of the zero axis is 0.2 milliseconds. Information theory stipulates that at least two samples must be taken in this time if the time interval is to be preserved (i.e. a sampling rate of 10kHz). However, if phase information is to be preserved as well, at least four samples are required (one every 50 microseconds). If a sampling period of 20 microseconds is considered, this is well within the capabilities of many relatively cheap 8 bit A/D convertors currently available.

The maximum time for which incoming data needs to be recorded is also found to be not more than 20 milliseconds. Therefore, at 8 bits every 20 microseconds, a total of 8000 bits may have to be processed to constitute one complete reading. This can be stored in a single 1K x 8 random access memory (RAM) integrated circuit.

Thus, both the amount of data required per reading, and the speed at which it has to be translated from analogue to digital form are well within the capabilities of present-day, low-cost integrated circuits.

The microprocessor control system

The fastest operation the microprocessor will be required to control is the A/D conversion. The full 8

bit conversion must be completed in 20 microseconds. With microprocessors now available running with clock rates of 4 or 6 megahertz this is not a difficult conversion time to achieve. But it would be better to connect the A/D converter as a parallel output to the microprocessor's 8 data lines rather than through a serial port.

A typical system

Dependent on the analytical skill of the operator, the system can take one of two forms :-

1) A minimum-control instrument with automatic read-out of just one or two results at a time.

2) A small hand-held microcomputer with push-button interface which would allow the operator to perform quick on-site analysis.

In either case the first requirement is the same - to digitise the accelerometer output signal and store it in a short-time memory. The broad outline of one suitable A/D converter has already been discussed. It should be capable of a 20 microsecond conversion to an 8-bit code over a 20 millisecond period (8000 bits).

Once the 8000 bits have been stored the microprocessor is capable of analysing that data in a variety of ways, dependent on the requirements of the vibration specialists. For instance, the frequency spectrum could be extracted: the time interval between direct and reflected pulse could be measured and translated directly into distance; (this would require the prior input of the type of material being investigated): phase angles and phase reversals could be measured giving possible data on the distances between different reflecting surfaces. In fact, any requirement of the vibration specialist could be catered for.

In some cases the analysis would take several seconds to perform, which might not be convenient for on-site systems. It would be up to the specialist to decide the balance between detailed analysis and on-site investigation time. With 8000 bits of information to be recorded at each measurement it would be difficult to take records of many points back to the laboratory. One 10 metre width of motorway, for instance, would require the recording of 80,000 bits; so even a 10 metre × 10 metre square would require nearly a million bits (taking into account the extra bits necessary, for example, for title, grid reference). Although systems are available with several megabits of storage capacity, such systems would only be used on sections of a structure of extra special interest and are outside the scope of these comments which are directed more towards "instant" analysis.

It would be possible to include a battery back-up RAM store of about 64,000 bits which could be used to record a few special waveforms for later analysis. Battery back-up RAMs can hold their contents for several months, but in this instance only a few hours would be necessary before the stored signals were transferred to the laboratory analysing equipment.

A schematic of one suitable system is shown in Figure 8. The accelerometer signal feeds through a buffer amplifier to the Analogue-to-Digital converter. This is controlled by timing pulses from the microprocessor so that the digital output is correctly synchronised to feed directly onto the processor's data bus. The processed data feeds into an 8K RAM as a short-term store. The buffer amplifier also feeds a trigger circuit which initiates the processor timing sequence.

Control signals from the instrument keyboard select the correct programme in the PROM so that the microprocessor manipulates the stored data and feeds appropriate information signals to the LCD matrix. If the data is sufficiently important, it can be transferred to one section of a 64K RAM on instruction from the keyboard.

In the simplified version the keyboard control to the PROM is either removed altogether or else reduced to one or two simple functions, and the PROM automatically selects a particular type of analysis when the A/D conversion is complete. The 64K RAM can probably be dispensed with too.

Figure 15 is a typical flow diagram. After "switch-on" the system resets to the "WAIT" state, with all possible systems powered down until a trigger pulse arrives from the accelerometer buffer amplifier. This starts the A/D conversion and 8K RAM storage. Then the first analysis programme is initiated and its result is fed to the LCD matrix. If any other analyses are required, they can either be initiated automatically in the simplified system, or initiated via the keyboard in the more complex system.

At the end of the analysis programmes the system returns to the "WAIT" state and powers down again.

It is envisaged that both simple and complex instruments will be hand-held ruggedised boxes with an LCD matrix display 252 on top. With reference to Figure 16, the complex instrument will probably have a decimal or hexadecimal keyboard 251 and an on/off switch 250, with a removable RAM 253 and charging socket 254.

The simple instrument would only be marginally cheaper than the complex instrument, the keyboard being replaced by one or two switches, and the 64K RAM being omitted.

The printed circuit board would ideally be the same for both models thereby halving layout costs. The positioning of components in each of the different cases would also be the same, with a few omissions for the simple instrument. Thus, the manufacturing costs of both models would be much the same, with the costs of tooling halved between them.

These comments also apply to the embodiment of Figure 17 wherein a quad operational amplifier 300 provides the active element of the signal acquisition and processing circuit. This circuit, together with a single 2 input Nand gate 301 and two monostables 302*a*, 320*b* controls a frequency meter module 303 which provides the read out. The monostables 302*a*, 302*b* are illustrated in Figure 17 as a single component 302. The left-hand side of component 302 comprises monostable 302*a*, whereas the right-hand side thereof comprises monostable 302*b*. The necessary "count" pulses are derived from an oscillator within the module 303 after dividing their frequency by 10 in divider 304. Power is derived from a single 9 volt battery 305, the voltage of which is controlled by

a voltage regulator 306 to provide a 5V positive supply. An inverter 307 produces a negative 5V supply. Low battery voltage is detected by a voltage sensor 308 which switches an astable connected integrated circuit timer 309 to drive a piezo electric warning sounder 310.

Circuit functioning

Incoming signals from the accelerometer are amplified by one quarter 300*a* of the quad operational amplifier. This is arranged as a conventional non-inverting amplifier with negative feed back. Two levels of gain are selectable by switch 311. The output of this amplifier is capacitively coupled by capacitor 312 to another quarter 300*b* of the amplifier 300 arranged as a conventional full wave rectifier with positive going output. A third quarter 300*c* of the amplifier 300 is arranged as a conventional integrator. The output of the fullwave rectifier is coupled to the inverting input of this integrator to produce at its output 313 a negative voltage of duration proportional to the amount of energy contained in the accelerometer signal 14. By applying positive feedback to the remaining quarter 300*d* of the amplifier 300 it is arranged to operate as a Schmitt trigger with preset trigger level. The negative output 313 of the integrator is directly connected to the inverting input of the Schmitt trigger 300*d*, causing the output 319 of the trigger to go positive if the input signals go more negative than the predetermined threshold level. Due to the hysteresis of the circuit, the input will have to rise slightly above the threshold for the output to return to low. This is desirable to prevent sporadic operation when the signal nears the threshold level.

The foregoing circuits provide a positive signal of nearly 5 volts for a duration proportional to the amount of energy content of the accelerometer signal 14. The remaining signal processing circuits are simply a means of measuring and displaying the length of this signal. The function of these circuits is as follows :-

A frequency meter module 303 is connected to function as an event counter. The module has an integral crystal oscillator 314 which is connected to divider 304 so as to produce output pulses at a certain frequency. These outputs are connected to one input of the two input Nand gate 301. The other input of the gate 301 is connected to the output 319 of the Schmitt trigger via a resistor 315. A diode 316 is included to stop negative excursions during switching, together with a stabilising resistor 317 and capacitor 318. The output of the Nand gate 301 is connected via capacitor 320 to the input of the event counter, i.e. module 303. Thus pulses at a rate of say 65,536 per second are applied to the counter (303) when an accelermoter signal of sufficient magnitude to operate the Schmitt trigger is received. However, for the counter to give a useful reading, its "reset" and "hold in" inputs must be controlled.

Two methods of counter control are provided, namely by selecting "0 sec" delay or, alternatively, by selecting "2 sec" delay using switch 322.

If set for 0 seconds delay, the input of the Nand gate 301 that is driven by the Schmitt trigger is connected to the input of the monostable 302*a* so that a short duration pulse is generated when the Schmitt trigger output goes high. The "reset" input 323 on the module 303 is connected to the output of this monostable so that the monostable goes from low to high for the duration of the pulse. Thus the counter (303) is reset at the start of each signal from the accelerometer and provides a fresh read-out for each signal (14) from the accelerometer. In this condition the "hold in" input 324 on the module 303 is connected to the output of the monostable 302*b* which has no input. As a result "hold in" input 324 remains low and is inhibited.

If counter control is set for 2 seconds delay, the input of the Nand gate 301 that is driven by the Schmitt trigger is connected to the input of monostable 302*b*, so that a 2 second (approx) pulse is generated when the Schmitt trigger output goes low. The output of this monostable is connected to the "hold in" input 324 of the module 303, thus "hold in" goes high, freezing the read-out for the duration of the pulse i.e. for about 2 seconds. However, the complementary output of the monostable 302*b* is in the 2 second delay select connected to the input of monostable 302*a*. As a result, at the end of the 2 second pulse, a short pulse from monostable 302*b* is applied to the "reset" input 323 on the module 303, and the counter is reset. At this instant no count is present so the display shows "00". Thus with delay set for 2 seconds the display will show "00" if no signals are being received from the accelerometer. When an accelerometer signal (14) is received, it will be displayed for about 2 seconds after which the read-out will return to "00". Signals received during the 2 second delay will not be displayed. This arrangement tends to reduce the chance to incorrect readings due to hammer bounce.

The embodiment of Figure 17 is provided with means for ensuring that sensing energy of a reflected pulse is delayed for a predetermined period, so as not to include all, or at least a significant part of the direct pulse.

Delay is achieved by the time constant of the capacitor 330 and the resistance 331, which determine the period during which the counter is held at zero (or datum) after the arrival of the first pulse received by the accelerometer. At the end of this period the output of the monostable 302*a* falls to zero, allowing the counter to start counting.

The invention can thus be used to evaluate the seriousness of a visible, (i.e. surface), crack :-

1. With the accelerometer sited on one side of the crack, take average readings resulting from impacts delivered to the surface, on the same side.

2. Leaving the accelerometer in position, switch the impacts to the opposite side of the crack, at substantially the same distance from the accelerometer as before, and note the average readings.

3. If the readings are similar the crack is insignificant. If no energy can pass across the crack, a zero reading will be obtained, indicating a very deep crack. If an intermediate value is obtained, this is directly proportional to the degree of cracking, as a substantially linear relationship exists between energy transfer and crack depth.

CLAIMS

1. A method of testing a structure comprising applying an energy pulse to the structure, and sensing energy of said pulse reflected from a fault in the structure.

2. A method as claimed in Claim 1, including the step of delaying the initiation of said sensing for a predetermined period after application of said energy pulse.

3. A method as claimed in Claim 1 or 2, wherein said sensing includes forming an electrical signal, integrating said signal, and displaying the integrated signal.

4. A method as claimed in Claim 3, wherein said electrical signal is used to obtain a time delay signal for causing said display to cease after a predetermined display time.

5. A method as claimed in Claim 3 or 4, wherein the electrical signal is produced by an accelerometer, the signal is rectified, the rectified signal is fed to a normally open switch device and to a first time-delay which after a first predetermined time triggers a second time-delay device to close the switch device, the second time-delay device opening the switch device after a second predetermined delay.

6. A method as claimed in Claim 5, wherein the rectified signal passes from the switch device through an integrator to a display meter through a further switch device.

7. A method as claimed in Claim 6, wherein the integrated signal passes to a third time-delay device arranged to open the further switch device after a predetermined time, and close the further switch device after a further predetermined time, closing of the further switch device being arranged to return the meter to a datum condition.

8. A method as claimed in any one of Claims 3 to 7, comprising deriving from said integrated signal a measure of the energy in the integrated signal.

9. A method as claimed in Claim 8, wherein the said measure is displayed digitally.

10. Apparatus for testing a structure, comprising means for applying an energy pulse to the structure, and means for sensing energy of said pulse reflected from a fault in the structure.

11. Apparatus as claimed in Claim 10, provided with means for delaying the operation of said sensing means for a predetermined period after said pulse is applied.

12. Apparatus as claimed in Claim 10 or 11, comprising accelerometer means for producing an output signal, integrator means operable so as to receive the output signal after a time delay and produce an integrated signal, and display meter means for displaying the integrated signal.

13. Apparatus as claimed in Claim 12, comprising switch means for receiving the integrated signal, time-delay means operable so as to open said switch means when said integrated signal has passed therethrough, and then to close said switch means after a predetermined time, said time-delay means being operable so as to be responsive to said integrated signal.

14. Apparatus as claimed in Claim 13, comprising further time-delay means operable so as to receive the output signal from the accelerometer means, normally open switch means operable so as to receive this signal, another time-delay means which after a first predetermined time controlled by the further time-delay means is energized by the further time-delay means and closes the switch means and then opens the switch means after a second predetermined time.

15. Apparatus as claimed in any one of Claims 11 to 14, wherein the meter means is operable to provide a digital display.

16. Apparatus as claimed in any one of Claims 11 to 15, including means for deriving from the integrated signal, a measure of the energy in the integrated signal.

17. Apparatus as claimed in Claim 14, 15 or 16, wherein the further time-delay means comprise comparator means.

18. Apparatus as claimed in Claim 14, 15, 16 or 17, comprising means for adjusting said another time-delay means so as to vary said second predetermined time.

19. Apparatus as claimed in any one pf claims 12 to 18, comprising means for storing said integrated signal, closing of said switch means and resetting said meter means to datum.

20. Apparatus as claimed in any one of Claims 12 to 19, wherein the integrator means is operable so that said integrated signal is of duration proportional to the energy of said accelerometer output signal.

21. Apparatus for testing a structure, comprising means for applying an energy pulse to the structure, means for sensing energy of said pulse reflected from a fault in the structure, and means for measuring the energy in said reflected pulse or in a predetermined period.

22. A method of testing a structure comprising applying an energy pulse to the structure, and sensing energy of said pulse reflected from a fault in the structure, said sensing of reflected energy comprising means for providing a measure of the energy in the reflected pulse or in a predetermined period.

23. A method of testing a structure, substantially as hereinbefore described with reference to Figures 1 to 17 of the accompanying drawings.

24. Apparatus for testing a structure, substantially as hereinbefore described with reference to Figures 1 to 17 of the accompanying drawings.

Printed in the UK for HMSO, D8818935, 7/84, 7102.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.